AMENDMENTS TO THE SPECIFICATION

Please replace the title beginning on page 1, line 5 as follows:

Technical Field ~~of the Invention~~

Please replace paragraph number 0001 with the following amended paragraph:

~~The present invention relates to a method~~ Methods of forming a copper wiring in a semiconductor device ~~and, more particularly, to a method of forming a copper wiring in a semiconductor device~~ are disclosed which are capable of preventing an electrical short condition between neighboring copper wirings and facilitating subsequent processes. The disclosed methods accomplish this through surface polishing, and by prohibiting electro-migration and stress migration of copper in the copper wiring formed within a damascene pattern.

Please replace paragraph number 0002 with the following amended paragraph:

Generally, as the semiconductor industry shifts to an ultra large-scale integration (ULSI) level, the geometry of the ~~device continues~~ devices continue to be narrowed to a sub-half-micron region. In view of improved performance and reliability, ~~the~~ circuit density is gradually increased. Copper has a high resistance to electro-migration (EM) since it has a higher melting point than aluminum. Thus, copper can improve reliability of the ~~device~~ devices. Further, copper can increase a signal transfer speed since it has a low resistivity. For this reason, in forming a metal wiring in a semiconductor device, copper has been used as an interconnection material useful for an integration circuit.

Please replace paragraph number 0003 with the following amended paragraph:

~~A method~~ Methods of burying copper that may be used currently ~~includes a~~ include physical vapor deposition (PVD) method/a reflow ~~method~~, ~~a~~ chemical vapor deposition (CVD) ~~method~~, ~~an~~ electroplating ~~method~~, ~~an~~ electroless-plating ~~method~~, and the like. Preferred methods ~~of them~~ are ~~the~~ electroplating ~~method~~ and ~~the~~ CVD ~~method~~, both of which have a relatively good copper burial characteristic.

Please replace paragraph number 0006 with the following amended paragraph:

Fig 1 is a sectional view for explaining the conventional method of forming the copper wiring ~~in the semiconductor device according to a prior art~~.

Please replace paragraph number 0008 with the following amended paragraph:

A copper anti-diffusion conductive film 15 is formed along the surface of the anti-polishing layer 13 including the damascene pattern 14. A copper layer is formed ~~enough~~ to sufficiently bury the damascene pattern 14. A CMP process is then performed until the anti-polishing layer 13 is exposed, thus forming a copper wiring 16 within the damascene pattern 14. Thereafter, a copper anti-diffusion insulating film 100 and a second interlayer insulating film 17 are formed on the entire structure including the copper wiring 16.

Please replace paragraph number 0009 with the following amended paragraph:

In the above-mentioned method, in order to prevent diffusion of copper elements from the copper wiring 16, ~~to the outside,~~ the copper wiring 16 is sealed using the copper anti-diffusion conductive film 15 and the copper anti-diffusion insulating film 100. In ~~the~~ a device having the copper wiring 16 formed by a conventional method, however, most of defective wirings are generated due to electro-migration and stress migration that take ~~takes~~ place at the interface between the copper anti-diffusion insulating film 100 and the copper anti-diffusion conductive film 15, as indicated by an arrow "A". This condition is caused by a lack in the bondability between the copper anti-diffusion insulating film 100 and the underlying layers 13, 15 and 16.

Please replace the title beginning on page 4, line 1 with the following:

SUMMARY OF THE ~~INVENTION~~ DISCLOSURE

Please replace paragraph number 0010 with the following amended paragraph:

~~The present invention is directed to provide a~~ A method of forming a copper wiring ~~in a semiconductor device~~ within a damascene pattern is disclosed which is capable of enhancing the electrical properties ~~of the device~~, preventing an electrical short ~~condition~~ between neighboring copper wirings and facilitating subsequent processes through surface polishing, by ~~prohibiting~~ preventing electro-migration and by preventing stress migration of copper in the copper wiring ~~formed within a damascene pattern~~.

Please replace paragraph number 0011 with the following amended paragraph:

According to a preferred embodiment, ~~of the present invention, there is provided~~ a disclosed method of forming a copper wiring ~~in a semiconductor device, including the steps of~~ comprises providing a substrate in which a damascene pattern is formed in an interlayer insulating film, forming a copper anti-diffusion conductive film and a copper layer on the entire structure including the damascene pattern, forming a copper wiring by means of a chemical mechanical polishing process, wherein the surface of the copper wiring is lower than the surface of the interlayer insulating film, and forming a copper anti-diffusion insulating film on the entire structure including the top of the copper wiring.

Please replace paragraph number 0012 with the following amended paragraph:

In the above method, the copper anti-diffusion insulating film ~~is~~ may be formed by covering materials such as methyl, benzochlorobutane, polyimide, arylether and hydrogen silsesquioxane, which contain Si, C and N in a type of a sol or gel, and then performing an annealing process in order to densify the covered film. In the above method, the annealing process ~~is~~ may be performed using an inert gas such as N_2, Ar, H_2 or He or a mixed gas of them at a temperature of 100 to 500°C.

Please replace the paragraph number 0013 with the following amended paragraph:

According to another embodiment, ~~of the present invention, there is provided a method~~ a method of forming a copper wiring ~~in a semiconductor device, including a first step of~~ comprises providing a substrate in which a damascene pattern is formed in an interlayer insulating film, a second step of forming a copper anti-diffusion conductive film and a copper layer on the entire structure including the damascene pattern, a third step of forming a copper wiring by means of a chemical mechanical polishing process, wherein the surface of the copper wiring is lower than the surface of the interlayer insulating film, and a fourth step of plasma-processing the surface of the copper wiring and then forming a selective copper anti-diffusion conductive film on the plasma-processed surface.

Please replace paragraph number 0014 with the following amended paragraph:

In the above method, the third step includes the steps of overly performing a chemical mechanical polishing process so that the top surface of the copper wiring is concaved and formed lower than the surface of the interlayer insulating film, and performing an annealing process so that the top surface of the copper wiring is changed from the concave shape to a convex shape while stabilizing the copper wiring.

Please replace paragraph number 0017 with the following amended paragraph:

Figs. 2A to 2C are sectional views for explaining a method of forming a copper wiring in a semiconductor device according to ~~an~~ one embodiment ~~of the present invention~~; and

Please replace paragraph number 0018 with the following amended paragraph:

Figs. 3A to 3C are sectional views for explaining a method of forming a copper wiring in a semiconductor device according to another embodiment ~~of the present invention~~.

Please replace the title beginning on page 6, line 14 as follows:

DETAILED DESCRIPTION OF THE ~~PRESENTLY~~ PREFERRED EMBODIMENTS

Please replace paragraph number 0019 with the following amended paragraph:

Now the preferred embodiments ~~according to the present invention~~ will be described with reference to the accompanying drawings. Since preferred embodiments are provided for the purpose ~~that the ordinary~~ of understanding for those skilled in the art, ~~are able to understand the present invention,~~ they may be modified in various manners and the scope of ~~the present invention~~ this disclosure is not limited by the preferred embodiments described ~~later~~ herein.

Please replace paragraph number 0020 with the following amended paragraph:

Figs. 2A to 2C are sectional views for explaining a disclosed method of forming a copper wiring in a semiconductor device ~~according to an embodiment of the present invention~~.

Please replace paragraph number 0027 with the following amended paragraph:

In the above, the first annealing process is performed in two methods. The first method is performed using an inert gas of N_2, Ar, H_2, or He, etc., or a mixed gas of them at a temperature range of 100 to 500°C. The second method is performed using an inert gas of N_2, Ar, H_2, or He, etc., or a mixed gas of them or in a vacuum state at a temperature range of 200 to 700°C for 5 or ~~lower~~ fewer minutes, preferably for 1 to 5 minutes in a rapid thermal annealing process.

Please replace paragraph number 0030 with the following amended paragraph:

In the above, the copper anti-diffusion insulating film 200 is formed using a material for which surface polishing can be easily performed, while having a copper anti-diffusion property. That is, the copper anti-diffusion insulating film 200 is formed by covering source materials such as methyl, benzochlorobutane, polyimide, arylether, hydrogen silsesquioxane, and the like, which contain Si, C, N, etc. in a type of a sol or gel having a good fluidity property, in a thickness of 300Å or more, preferably in the range of 300 to 700°C by means of a spin-on deposition mode, and then performing a second annealing process to densify the covered film. In this case, the second annealing process is performed in two methods. The first method is performed using an inert gas of N_2, Ar, H_2, He, etc., or a mixed gas of them at a temperature range of 100 to 500°C, for 1 or more ~~minute~~ minutes, preferably 1 to 5 minutes. The second method is performed in a vacuum state at a temperature range of 100 to 500°C for 1 or ~~over~~ more minutes, preferably for 1 to 5 minutes.

Please replace paragraph number 0032 with the following amended paragraph:

Figs. 3A to 3C are sectional views for explaining ~~a~~ another method of forming a copper wiring in a semiconductor device ~~according to another embodiment of the present invention~~.

Please replace paragraph number 0038 with the following amended paragraph:

By reference to Fig. 3B, an annealing process is performed to stabilize the copper wiring 36. In ~~the~~ this case, the top surface of the copper wiring 36 is changed from the concave shape to a convex shape so as to minimize surface energy due to heat.

Please replace paragraph number 0039 with the following amended paragraph:

In the above, the annealing process is performed in two methods. The first method is performed using an inert gas of N_2, Ar, H_2, He, etc. or a mixed gas of them at a temperature range of 100 to 500°C. The second method is performed using an inert gas of N_2, Ar, H_2, He, etc. or a mixed gas of them or in a vacuum state at a temperature range of 200 to 700°C for 5 or ~~lower~~ fewer minutes, preferably for 1 to 5 minutes in a rapid thermal annealing process.

Please replace paragraph number 0040 with the following amended paragraph:

With reference to Fig. 3C, in order to remove impurities such as an oxide layer generated on the surface of the copper wiring 36, plasma is processed and a selective copper anti-diffusion ~~insulating~~ conductive film 300 is formed on the entire structure including the top surface of the copper wiring 36 having the convex shape. A second interlayer insulating film 37 is then formed on the entire structure including the copper anti-diffusion ~~insulating~~ conductive film 300.

Please replace paragraph number 0044 with the following amended paragraph:

According to ~~one~~ the first embodiment ~~of the present invention~~ described above, a copper anti-diffusion insulating film is formed not only within a damascene pattern but also on the entire structure, thus serving as a barrier to prohibit electro-migration and stress migration of copper. It is thus possible to improve reliability of a wiring. Furthermore, the whole plane including an upper side of a copper wiring is polished without a step to facilitate a photolithography process, an etch process, etc. that are subsequent performed. It is therefore possible to improve reliability in process.

Please replace paragraph number 0045 with the following amended paragraph:

According to ~~another~~ the second embodiment ~~of the present invention~~ described above, the top surface of a copper wiring is lower than the surface of an interlayer insulating film of a low dielectric constant neighboring it and a selective copper anti-diffusion conductive film on the copper wiring is formed within a damascene pattern without

causing a step with an interlayer insulating film of a dielectric constant neighboring it. As the selective copper anti-diffusion conductive film serves as a barrier to prohibit electro-migration and stress migration of copper, it is possible to improve reliability of the wiring. Furthermore, the selective copper anti-diffusion conductive film is formed only within the damascene pattern to prevent an electrical short condition among neighboring copper wirings. It is thus possible to improve wiring fail. Therefore, the present invention has advantages that it can enhance electrical properties and reliability of devices and makes it possible to realize higher-integration of the device.

Please replace paragraph number 0046 with the following amended paragraph:

Although the foregoing description has been made with reference to the preferred embodiments, it is to be understood that changes and modifications of the ~~present invention~~ disclosed methods may be made by the ordinary skilled in the art without departing from the spirit and scope of ~~the present invention~~ this disclosure and the appended claims.